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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,751	03/10/2004	Giao Minh Pham	005510.P081	6419

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/798,751	PHAM, GIAO MINH	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13-16* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Roy et al. (USP 6388495).

Roy et al. discloses in figure 6 a circuit, comprising: a first current limiting circuit (120) coupled between a selector terminal (105) and a first voltage bus (Vdd), the first current limiting circuit adapted to vary a current limit out of the selector terminal in response to a voltage on the selector terminal; and a second current limiting circuit (155) coupled between the selector terminal and a second voltage bus (115), the second current limiting circuit adapted to vary a current limit into the selector terminal in response to the voltage on the selector terminal.

3. Claims 1-10 and 13-16 are rejected under 35 U.S.C. 102(b) as being anticipated by Lam et al. (USP 5856760).

As to claim 1, Lam et al. discloses in figure 5 a circuit, comprising: a first current limiting circuit (50) coupled between a selector terminal (24) and a first voltage bus (+Vcc), the first current limiting circuit adapted to vary a current limit out of the selector terminal in response to a voltage on the selector terminal; and a second current limiting circuit (52) coupled between the selector terminal and a second voltage bus (-Vee), the second current limiting circuit adapted to vary a current limit into the selector terminal in response to the voltage on the selector terminal.

As to claim 2, figure 5 shows a plurality of voltage comparators (Q4, Cs2 and Q3, CS1) coupled to the selector terminal.

As to claim 3, figure 5 shows a decoder circuit (Q5, Q6) coupled to the plurality of voltage comparators.

As to claim 4, figure 5 shows that the first current limiting circuit includes a first switch (Q1) and a first variable current source (58) coupled between the first voltage bus the selector terminal.

As to claim 5, figure 5 shows that the first switch is adapted to conduct when the voltage on the selector terminal is below a first threshold voltage *(the first threshold is equal to voltage at the base of transistor Q1 minus the threshold of transistor Q1)*, the first switch is adapted not to conduct when the voltage on the selector terminal is above a second threshold voltage (the second threshold voltage is the voltage at the base of transistor Q1).

As to claim 6, figure 5 shows that the second current limiting circuit includes a second switch (Q2) and a second variable current source (64) coupled between the selector terminal and the second voltage bus.

As to claim 7, figure 5 shows that the second switch is adapted to conduct when the voltage on the selector terminal is above a third threshold voltage (the third threshold voltage is equal to the voltage at the base of transistor Q2 add the threshold voltage of transistor Q2), the second switch is adapted not to conduct when the voltage on the selector terminal is below a fourth threshold voltage (the second threshold voltage is equal to the voltage at the base of transistor Q2).

As to claim 8, figure 5 shows that the first current limiting circuit is adapted to vary the current limit out of the selector terminal to a first current limit when the voltage on the selector terminal is below a fifth threshold voltage (fifth threshold voltage is a voltage that low enough to turn on transistor Q3), the first current limiting circuit is adapted to vary the current limit out of the selector terminal to a second current limit when the voltage on the selector terminal is above a sixth threshold voltage (sixth threshold voltage is a voltage that is high enough to turn off transistor Q3).

As to claim 9, figure 5 shows that the second current limiting circuit is adapted to vary the current limit into the selector terminal to a third current limit when the voltage on the selector terminal is above a seventh threshold voltage (the seventh threshold voltage is a voltage that is high enough to turn on transistor Q4), wherein the second current limiting circuit is adapted to vary the current limit into the selector terminal to a fourth current limit when the voltage on the selector terminal is below an eighth threshold voltage (eighth threshold voltage is a voltage that is low enough to turn off transistor Q4).

As to claim 10, it is inherent that the first and second threshold voltages is less than the third and fourth voltages.

As to claim 13, figure 5 shows that the first current limit is less than the second current limit. *When transistor Q3 is on, transistor Q8 is off. Transistor Q1 generates the first current limit which is determined by the voltage at the base of transistor Q1. when transistor Q3 is off, transistor Q8 is on, transistor Q1 generates the second current limit. The voltage at the base of transistor Q1 is higher when transistor Q 8 is on. Thus, the second current limit is greater than the first current limit.*

As to claim 14, figure 5 shows that the third current is less than the fourth current (similar season explained in the rejection of claim 13).

As to claim 15, figure 5 shows that the circuit further included in an integrated circuit.

As to claim 16, figure 5 shows that the integrated circuit device is a controller in a switching power supply (Vout).

Allowable Subject Matter

4. Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 11 and 12 would be allowable because the prior art fails to teach or suggest that the fifth and sixth threshold voltages are lower than the first and second threshold voltages, or the seventh and eighth threshold voltages are higher than the third and fourth threshold voltages.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. These references are cited as interest because they show some circuits analogous to the claimed invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

May 31, 2005